CLAIMS:

1. A process for forming a semiconductor product, comprising the steps of:

providing a semiconductor substrate having a semiconductor surface;

introducing N-type dopant impurities into said semiconductor surface, thereby forming N-doped regions within said semiconductor surface;

introducing nitrogen into at least one of said N-doped regions to form at least one nitrogen region; and,

thermally oxidizing said substrate surface to form an oxide film on said semiconductor surface, said oxide film having a first thickness in said at least one nitrogen region and a second thickness being greater than said first thickness in other portions of said N-doped regions.

2. The process as in claim 1, in which said semiconductor product is a Metal Oxide Semiconductor (MOS) capacitor and in which each nitrogen region forms a capacitor region and further comprising forming a top capacitor plate of one of a conductive material and a semiconductor material over each capacitor region, after said step of thermally oxidizing.

3. The process as in claim 1, in which said step of introducing nitrogen comprises ion implantation.

4. The process as in claim 3, in which said step of introducing nitrogen includes an implant energy within the range of 5-9 keV and an implant dosage which lies within the range of $10^{14}/cm^2$ to $10^{15}/cm^2$.

5. The process as in claim 1, in which said step of thermally oxidizing includes forming said oxide film having said first thickness being less than 50% of said second thickness.

6. The process as in claim 1, in which said first thickness is less than 55 angstroms and said second thickness lies within the range of 80-150 angstroms.

7. The process as in claim 1, in which said step of introducing N-type dopant impurities includes forming said N-doped regions to include an N-type impurity concentration which lies within the range of $10^{18}/cm^3$ to $10^{19}/cm^3$.

8. The process as in claim 1, in which said nitrogen region includes a nitrogen density within the range of 10^{17} to $10^{19}/cm^3$.

9. The process as in claim 1, in which semiconductor surface regions in which said N-type dopant impurities are not introduced, are designated undoped regions, and said step of thermally oxidizing includes forming said oxide film having a third thickness in said undoped regions, said third thickness being less than 50% of said second thickness.

10. The process as in claim 1, further comprising the step of defining said at least one nitrogen region prior to said step of introducing nitrogen, said defining comprising forming a masking pattern in a photosensitive material.

11. The process as in claim 10, in which said masking pattern includes each nitrogen region forming a lower capacitor electrode, having a rectangular shape and including sides ranging from 2 to 100 microns in length.

12. The process as in claim 1, wherein said thermally oxidizing comprises furnace oxidation at a temperature ranging from 750°C to 950°C, for a time ranging from 5 to 15 minutes.

13. The process as in claim 1, wherein said N-type dopant impurity comprises one of phosphorous and arsenic.

14. The process as in claim 1, in which said step of introducing nitrogen comprises introducing nitrogen into at least one entire N-doped region of said N-doped regions.

15. The process as in claim 1, in which said step of introducing nitrogen includes introducing nitrogen into a first portion of a designated N-doped region, a second portion of said designated N-doped region not having nitrogen introduced therein.

16. The process as in claim 1, wherein said semiconductor substrate comprises silicon and said oxide film comprises silicon dioxide.

17. A process for forming a thermal oxide film having multiple thicknesses, comprising the steps of:

providing a silicon substrate having a silicon surface;

forming a plurality of dopant impurity regions in said silicon surface, said dopant impurity regions formed of one of phosphorous and arsenic;

implanting nitrogen into a nitrogen portion of at least one of said dopant impurity regions; and

thermally oxidizing said substrate to form an oxide film thereover, said oxide film having a first thickness in said nitrogen portions and a second thickness in other portions of said dopant impurity regions, said second thickness being greater than said first thickness by at least 80%.

18. The process as in claim 17, in which said step of thermally oxidizing includes forming said oxide film having a third thickness in undoped regions of said silicon surface, said third thickness and said first thickness being substantially equal.

19. A process for forming a Metal Oxide Semiconductor (MOS) capacitor, comprising the steps of:

providing a silicon substrate having a silicon surface;

introducing N-type dopant impurities into said silicon surface, thereby forming N-doped regions within said silicon surface;

implanting nitrogen into at least one of said N-doped regions to form at least one capacitor region;

thermally oxidizing said substrate to form an oxide film on said silicon surface, said oxide film having a first thickness in said at least one capacitor region and a

second thickness being greater than said first thickness in other portions of said N-doped regions; and,

forming a top capacitor plate of at least one of a conductive material and a semiconductor material over said at least one capacitor region.

20. A semiconductor product including a capacitor formed over an N-type impurity region of a semiconductor substrate, said capacitor comprising an upper electrode, a lower electrode formed of a capacitor portion of said N-type impurity region which further includes nitrogen therein, and a dielectric interposed between said upper and lower electrodes, said dielectric including nitrogen therein.

21. The semiconductor product as in claim 20, in which said capacitor portion of said N-type impurity region includes a nitrogen concentration within a range of $10^{17}/cm^3$ to $10^{19}/cm^3$, and said N-type impurity region includes an N-type dopant impurity concentration ranging from $10^{18}/cm^3$ to $10^{19}/cm^3$.

22. The semiconductor product as in claim 20, in which said semiconductor substrate comprises silicon and said dielectric film comprises a thermal oxide film further extending over further portions of said N-type impurity region and over bulk portions of said silicon substrate in which N-type impurities are not present, said thermal oxide film characterized by having a first thickness in said capacitor region being less than a second thickness over said further portions of said N-type impurity region, and a third thickness over said bulk portions being substantially the same as said first thickness.

23. The semiconductor product as in claim 20, in which said dielectric film is a continuous film which further extends over further portions of said N-type impurity region and over bulk portions of said substrate in which N-type impurities are not present, said dielectric film characterized by the absence of nitrogen in regions other than said capacitor region.

24. The semiconductor product as in claim 23, wherein said dielectric film comprises a thermal oxide film.

25. A semiconductor product including a capacitor formed over a silicon substrate and including a lower electrode formed of a region of said silicon substrate including nitrogen and N-type impurities therein.

26. The semiconductor product as in claim 25, in which said capacitor includes a capacitor dielectric being an oxide film including nitrogen therein.